REMARKS/ARGUMENTS

Claims 2-21 are pending. Claims 2, 6, 12, and 16 have been amended. No new matter has been introduced. Applicants believe the claims comply with 35 U.S.C. § 112.

Claims 2-21 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. No. 6,359,978 to Kobayashi et al. in view of U.S. No. 5,568,633 to Boudou et al. The Examiner recognizes that Kobayashi et al. does not teach that the local memory and the cache memory store management information that is used exclusively by at least one microprocessor and exclusive of information used by any other microprocessor, but cites Boudou et al. for allegedly disclosing this feature.

Claims 2-5

Applicants respectfully submit that independent claim 2 is patentable over Kobayashi et al. and Boudou et al. because, for instance, they do not teach or suggest a local memory for a control program and for in-memory management information and not for the user data; and that the local memory and the cache memory store management information that is used only by the at least one microprocessor, and the local memory and the cache memory are exclusive of management information that is used by any microprocessor other than the at least one microprocessor.

Kobayashi et al. discloses that both common memories 12a and 12b have the same content including user data. Boudou et al. is cited merely for allegedly disclosing that the local memory and the cache memory store management information that is used exclusively by at least one microprocessor and exclusive of information used by any other microprocessor. Boudou et al. does not cure the deficiency of Kobayashi et al., in that it also fails to teach or suggest that the local memory is not used for the user data.

Boudou et al. merely discloses a block processed by a processor 2.11. It does not teach user data that are exchanged between a host system and a data storage unit. Nor does it teach a cache memory for the user data and the in-cache management information. Indeed, Boudou et al. does not even disclose different types of data (i.e., user data and management information).

Moreover, Kobayashi et al. and Boudou et al. cannot be combined in the manner indicated by the Examiner due to their conflicting teachings. Kobayashi et al. discloses that both common memory 12a and 12b have user data and management information. In contrast, Boudou et al. discloses only a block processed by a processor 2.11, and fails to teach the user data that are exchanged between a host system and a data storage unit.

For at least the foregoing reasons, claim 2 and claims 3-5 depending therefrom are patentable over Kobayashi et al. and Boudou et al.

Claims 6-11

Applicants respectfully assert that independent claim 6 is patentable over Kobayashi et al. and Boudou et al. because, for instance, they do not teach or suggest a cache memory for user data that is transferred between the host computer and the storage units; and that the local memory and the cache memory store management information that is used only by the at least one processor, the local memory and the cache memory are exclusive of management information that is used by any processor other than the at least one processor, and the local memory does not store the user data.

As discussed above, Kobayashi et al. discloses that both common memories 12a and 12b have the same content including user data, and Boudou et al. does not cure the deficiency of Kobayashi et al. Boudou et al. does not even disclose different types of data (i.e., user data and management information). While Kobayashi et al. discloses that both common memory 12a and 12b have user data and management information, Boudou et al. discloses only a block processed by a processor 2.11, and fails to teach the user data that are exchanged between a host system and a data storage unit. Therefore, Kobayashi et al. and Boudou et al. cannot be combined in the manner indicated by the Examiner due to their conflicting teachings.

For at least the foregoing reasons, claim 6 and claims 7-11 depending therefrom are patentable over Kobayashi et al. and Boudou et al.

Claims 12-15

Applicants respectfully submit that independent claim 12 is patentable over Kobayashi et al. and Boudou et al. because, for instance, they do not teach or suggest a cache memory for user data being transferred between the host computer and the storage units, the cache memory storing management information relating to user data that is stored in the cache memory; and that the local memory and the cache memory store management information that is used only by the at least one processor, the local memory and the cache memory are exclusive of management information that is used by any processor other than the at least one processor, and the local memory does not store the user data.

As discussed above, Kobayashi et al. discloses that both common memories 12a and 12b have the same content including user data, and Boudou et al. does not cure the deficiency of Kobayashi et al. Boudou et al. does not even disclose different types of data (i.e., user data and management information). While Kobayashi et al. discloses that both common memory 12a and 12b have user data and management information, Boudou et al. discloses only a block processed by a processor 2.11, and fails to teach the user data that are exchanged between a host system and a data storage unit. Therefore, Kobayashi et al. and Boudou et al. cannot be combined in the manner indicated by the Examiner due to their conflicting teachings.

For at least the foregoing reasons, claim 12 and claims 13-15 depending therefrom are patentable over Kobayashi et al. and Boudou et al.

Claims 16-21

Applicants respectfully contend that independent claim 16 is patentable over Kobayashi et al. and Boudou et al. because, for instance, they do not teach or suggest a cache memory for temporarily storing data transferred between the host computer and the storage units and for storing management information relating to user data that is stored in the cache memory; and that the local memory and the cache memory store management information that is used only by the at least one processor, the local memory and the cache memory are exclusive of management information that is used by any processor other than the at least one processor, and the local memory does not store the user data.

As discussed above, Kobayashi et al. discloses that both common memories 12a and 12b have the same content including user data, and Boudou et al. does not cure the deficiency of Kobayashi et al. Boudou et al. does not even disclose different types of data (i.e., user data and management information). While Kobayashi et al. discloses that both common memory 12a and 12b have user data and management information, Boudou et al. discloses only a block processed by a processor 2.11, and fails to teach the user data that are exchanged between a host system and a data storage unit. Therefore, Kobayashi et al. and Boudou et al. cannot be combined in the manner indicated by the Examiner due to their conflicting teachings.

For at least the foregoing reasons, claim 16 and claims 17-21 depending therefrom are patentable over Kobayashi et al. and Boudou et al.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance and an action to that end is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,

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